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TOPIC:

Koomey's law and the steep subthreshold transistors – What is in store?

ABSTRACT:

For too long the semiconductor industry has been working hard to put increased computational power in the same chip area. This has led to forceful scaling of transistors approaching their fundamental limits. For energy efficient computing, supply voltage too needs to be aggressively scaled down. However, at these nanoscale dimensions, conventional MOSFETs are not pliable to voltage scaling since their subthreshold swing cannot get below 60 mV/decade. This has led to the search for steep subthreshold transistors. Two alternate device structures have emerged as possible substitutes for the conventional MOSFETs. Both these devices are gated P-i-N structures, known as the tunnel field effect transistor (TFET) and the impact-ionization MOSFET (IMOS). The TFET is particularly important for low power applications while the IMOS exhibits extremely low subthreshold swings. However, both the devices need to be optimized. The problem with TFETs is their low ON-state current and with IMOS, its large supply voltage. During the last few years, there have been tremendous efforts in understanding the working of TFETs and IMOS to optimize their performance. This talk is introductory in style but will provide a comprehensive view of the recent innovations that have been introduced and will also highlight the future challenges that need to be overcome.

PROFILE:

M. Jagadesh Kumar is currently the NXP (Philips) Chair Professor established at IIT Delhi by Philips Semiconductors, The Netherlands. He is the chief investigator of the Nano Research Facility being built at IIT Delhi. His research interests include nanoelectronic devices, innovative device design for nanoscale applications, integrated-circuit technology, and power semiconductor devices. He has published more than 180 papers in the above areas. He received the 2013 Award for Excellence in Teaching (in large class category) from IIT Delhi.

Dr. Kumar is a Fellow of the Indian National Academy of Engineering, The National Academy of Sciences, India and the Institution of Electronics and Telecommunication Engineers (IETE), India. He is recognized as a Distinguished Lecturer of the IEEE Electron Devices Society (EDS). He is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES. He was a recipient of the 29th IETE Ram Lal Wadhwa Gold Medal for his distinguished contribution in the field of semiconductor device design and modeling. He was also the first recipient of the India Semiconductor Association–VLSI Society of India TechnoMentor Award given by the India Semiconductor Association to recognize a distinguished Indian academician for playing a significant role as a Mentor and Researcher. He is also a recipient of the 2008 IBM Faculty Award.